What is Claimed is:

1. A pumping voltage generator, comprising:

a detector configured to detect a plurality of pumping voltage levels, and to output a plurality of enable signals in response to the detected voltage levels;

a cycle selecting unit configured to output an oscillation cycle selecting signal for controlling an oscillation cycle of a pumping voltage in response to the plurality of enable signals;

an oscillator configured to be enabled by one of the plurality of enable signals, and to output an oscillation signal corresponding to the oscillation cycle selecting signal;

a control driver configured to output a pumping control signal for controlling the pumping operation in response to the oscillation signal; and

a pumping unit configured to output the pumping voltage in response to the pumping control signal.

2. The generator of claim 1, wherein the detector comprises:

a voltage divider configured to connect a plurality of resistances in series between a power voltage and a

ground voltage, and to divide a voltage and output the voltage through a first node and a second node among the resistances;

a first differential amplifier unit configured to compare a reference voltage with an output voltage from the first node, and to output a first enable signal among the plurality of enable signals; and

a second differential amplifier unit configured to compare the reference voltage with an output voltage from the second node, and to output a second enable signal among the plurality of enable signals.

3. The generator of claim 2, wherein the output voltage of the first node is higher than that of the second node.

4. The generator of claim 1, wherein the cycle selecting unit comprises:

a pulse generator configured to receive one of the plurality of enable signals, and to output a predetermined pulse; and

an oscillation cycle selecting signal output unit configured to output the oscillation cycle selecting signal for selecting an oscillation cycle by using the

predetermined pulse and the plurality of enable signals.

5. The generator of claim 4, wherein the pulse generator comprises:

a plurality of inverter chains configured to be connected in series, and to delay one of the plurality of enable signals; and

a logic means configured to logically operate the enable signal delayed by the inverter chain, and to output the predetermined pulse.

6. The generator of claim 4, wherein the oscillation cycle selecting signal output unit comprises:

a first enable input means configured to be controlled by the pulse signal, and to receive a first enable signal of the plurality of enable signals;

a second enable input means configured to be controlled by the pulse signal, and to receive a second enable signal of the plurality of enable signals; and

a logic means configured to logically operate output signals from the first enable input unit and the second enable input unit with the first enable signal.

7. The generator of claim 6, wherein the first

enable input means comprises:

a first inverter means configured to invert the first enable signal;

a first transistor means configured to have a drain connected to an output terminal of the first inverter, and to be controlled by the pulse;

a latch means configured to have one terminal connected to a source of the first transistor, and to latch an output signal from the first inverter;

a second inverter means configured to invert the pulse; and

a second transistor means configured to have a drain connected to the other terminal of the latch means and a source connected to an input terminal of the logic means, and to be controlled by an output signal from the second inverter.

8. The generator of claim 6, wherein the second enable input unit comprises:

a first inverter means configured to invert the first enable signal;

a first transistor means configured to have a drain connected to an output terminal of the first inverter, and to be controlled by the pulse;

a latch means configured to have one terminal connected to a source of the first transistor, and to latch an output signal from the first inverter;

a second inverter means configured to invert the pulse; and

a second transistor means configured to have a drain connected the other terminal of the latch means and a source connected to an input terminal of the logic means, and to be controlled by an output signal from the second inverter.

9. The generator of claim 6, wherein the logic means is a NAND gate.

10. The generator of claim 1, wherein the oscillator comprises:

an inverter chain configured to included a plurality of inverters connected in series, wherein an output signal of each inverter is controlled by the oscillation cycle selecting signal; and

a logic operation means configured to logically operate one of the plurality of enable signal with an output signal from the inverter chain, and to output the logic operation result into an input terminal of the

inverter chain.

11. The generator of claim 10, wherein an inverter in the inverter chain comprises:

an oscillation cycle selecting signal input unit configured to receive the oscillation cycle selecting signal, to perform a predetermined delay operation and a logic operation on the received signal, and to output the operation result;

an inverter input unit configured to receive an output signal from the previous inverter, to perform a predetermined delay operation and a logic operation on the received signal, and to output the operation result;

an inverter output unit configured to be controlled by output signals from the oscillation cycle selecting signal input unit and the inverter input unit, and to output a predetermined logic signal..

12. The generator of claim 11, wherein the oscillation cycle selecting signal input unit comprises:

an inverter means configured to invert the oscillation cycle selecting signal;

a NAND gate configured to NAND output signals from the inverter means and the previous inverter; and

a NOR gate configured to NOR the oscillation cycle selecting signal and an output signal from the NAND gate.

13. The generator of claim 11, wherein the inverter input unit comprises:

a NAND gate configured to be controlled by a power voltage, and to invert an output signal from the previous inverter;

an inverter means configured to invert an output signal from the NAND gate; and

a NOR gate configured to be controlled by a ground voltage, and to invert an output signal from the inverter means.

14. The generator of claim 11, wherein the inverter input unit comprises:

a first PMOS transistor configured to be controlled by an output signal from the oscillation cycle selecting signal input unit, and to output a high level signal if turned on;

a second PMOS transistor configured to be controlled by an output signal from the inverter input unit, and to output a high level signal if turned on; and

a NMOS transistor configured to be controlled by an

output signal from the inverter input unit, and to output a low level signal if turned on.